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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/828,556	04/05/2001	Anthony P. Mauro	010034	6493

23696 7590 09/24/2004

Qualcomm Incorporated
Patents Department
5775 Morehouse Drive
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EXAMINER	
NORRIS, TREMAYNE M	

ART UNIT	PAPER NUMBER
2137	

DATE MAILED: 09/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/828,556	MAURO ET AL.	
	Examiner	Art Unit	
	Tremayne M. Norris	2137	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/15/02; 4/02/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-5, 7-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Krishna et al (WO 0105086).

Regarding claim 1, Krishna teaches A device for accelerating functioning of a software application having multi-layer, high overhead protocols, the device comprising:

a first processor operating a software application having a multi-layer protocol (page 2 lines 3-11; page 6 lines 22-26);

a high performance processor configured to operate one layer of the multi-layer protocol according to a command from the first processor (page 3 lines 2-25); and

a memory accessible to each of the first processor and the high performance processor for passing commands and data between the first processor and the high performance processor (page 7 lines 23-26; page 8 lines 22-29).

Regarding claim 2, Krishna teaches the first processor operates a multi-layer security protocol (page 2 lines 3-11; page 3 lines 2-14).

Regarding claim 3, Krishna teaches the high performance processor is configured to operate a mathematical algorithm layer of the multi-layer protocol (page 3 lines 15-25: cryptography algorithms).

Regarding claim 4, Krishna teaches the high performance processor further comprises a digital signal processor (page 1 lines 7-21; page 3 lines 2-14).

Regarding claim 5, Krishna teaches the digital signal processor is further configured to operate a modular math function (page 3 lines 15-25: cryptography algorithms).

Regarding claim 7, Krishna teaches a device for accelerating security protocols, the device comprising;

a multi-layer security protocol having one or more of an encryption algorithm and an authentication algorithm (page 2 lines 3-11);

a shared memory (page 7 lines 23-26; page 8 lines 22-29);

a processor coupled to the memory and operating a first portion of a predetermined one of the security protocols (page 2 lines 3-11; page 6 lines 22-26); and

a high performance processor coupled to the memory and operating a second portion of the predetermined one of the security protocols (page 3 lines 2-25).

Regarding claim 8, Krishna teaches the high performance processor operates the second portion of the security protocol in response to a command from the processor and returns an interrupt signal (page 15 lines 30-33).

Regarding claim 9, Krishna teaches the high performance processor operates the second portion of the security protocol on data from the processor (page 3 lines 2-25).

Regarding claim 10, Krishna teaches the high performance processor operates the second portion of the security protocol using a modular math function (page 3 lines 15-25: cryptography algorithms).

Regarding claim 11, Krishna teaches the processor passes the data to the high performance processor via the shared memory, and the high performance processor returns a result from operating the second portion of the security protocol to the processor via the shared memory (page 8 lines 17-29; page 15 lines 25-34).

Regarding claim 12, Krishna teaches a circuit for partitioning a multi-layer security services protocol, the circuit comprising:

a shared memory (page 7 lines 23-26; page 8 lines 22-29);

first (page 2 lines 3-11; page 6 lines 22-26) and second processor (page 3 lines 2-25) cores coupled to the shared memory ;

a multi-layer security services protocol partitioned between each of the first and second processor cores page 2 lines 3-11;

one or more application program interfaces operated by the first processor core for interfacing between the security services protocol and the second processor core (page 6 lines 19-20); and

a modular math function operating on the second processor core (page 3 lines 15-25: cryptography algorithms).

Regarding claim 13, Krishna teaches the first and second processor cores are coupled together through the shared memory (page 6 lines 22-24; page 7 lines 23-33).

Regarding claim 14, Krishna teaches the security services protocol further comprises one of an encryption algorithm and an authentication algorithm (page 9 lines 1-7).

Regarding claim 15, Krishna teaches a method for accelerating a multi-layer protocol, the method comprising:

partitioning a function of a multi-layer protocol in a first processor (page 2 lines 3-11; page 6 lines 22-26);

distributing the function to a second high performance processor via a memory shared by both the first and second processors (page 7 lines 23-26; page 8 lines 22-29);

performing the distributed function in the high performance processor (page 3 lines 2-25); and

returning a result of the distributed function from the high performance processor via the shared memory (page 8 lines 17-29; page 15 lines 25-34).

Regarding claim 16, Krishna teaches the distributed function further comprises performing the distributed function in response to a command from a first processor (page 3 lines 2-25; page 8 lines 10-16; page 9 lines 1-7).

Regarding claim 17, Krishna teaches the first processor performs the partitioning of the function (page 15 lines 8-15).

Regarding claim 18, Krishna teaches performing the distributed function comprises operating an algorithm to perform the function (page 3 lines 15-25: cryptography algorithms).

Regarding claim 19, Krishna teaches the algorithm is a modular math function (page 3 lines 15-25: cryptography algorithms).

Regarding claim 20, Krishna teaches the multi-layer protocol is a security layer (page 2 lines 3-11).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Krishna.

Regarding claim 6, the examiner takes official notice that modular exponentiation used for encryption is well known in the cryptography art. It would have been obvious to one of ordinary skill in the art to incorporate exponential functions in order to enhance throughput by increasing processing speed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tremayne M. Norris whose telephone number is (571)

272-3874. The examiner can normally be reached on M-F 7:30AM-5:00PM alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Caldwell can be reached on (571) 272-3868. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tremayne Norris

September 9, 2004

Andrew Caldwell

Andrew Caldwell